REMARKS

Claims 1-4, 6-16 and 18-24, rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,789,242 (LIU) are canceled and replaced with new claims 25-43, which are patentable over LIU for reasons discussed below.

Claim 25

A typical digital circuit includes a set of clocked storage elements (registers, latches, flip-flops and the like), unclocked logic elements (NAND gates, OR gates, etc) that communicate through signals. A circuit simulator determines the behavior of the output signals of the storage and logic elements in response to circuit input signals. When viewing simulation results, a designer will often want to first look at the states of signals appearing at the outputs of the clocked storage elements at a succession of discrete times during the simulation at which the storage elements are clocked to determine whether these signals are of expected states. When the designer finds that one of those output signals of a storage element (a "first signals") is of an unexpected state at some particular one of the discrete times (a "first discrete time"), the designer wants to figure out why. To do so, the designer might first like to determine a first set of all storage element output signals or circuit input signals at a "second discrete time" immediately proceeding the first discrete time that can influence the state of the first signal at the first discrete time.

When all of the signals of the first set are of the correct state at the second discrete time, then the designer might conclude that there is an error in the logic that processes the signals of the first set to produce the first signal, and can thereafter review the schematic diagram for that portion of the circuit.

On the other hand, if one particular signal of the second set is of an incorrect state at the second discrete time, the designer might conclude that the error in the first signal state may have arisen from an error in the logic that produced that particular signal of the second set, and occurred some time before the second discrete time.

LIU describes a system for generating a display to help a user debug a circuit design. When the user selects a particular signal of the circuit at a particular discrete time, and selects a particular

time interval leading up to that discrete time, LIU's system displays a "temporal schematic diagram" as illustrated in LIU's FIG. 5. Here the user has selected the output signal of storage element 307 at a discrete time t8 and has selected the time interval t5-t8. The temporal schematic diagram includes a separate area for each discrete time t5-t8 containing a schematic diagram of all circuit elements producing output signals at the corresponding discrete time that affect the state of the output signal of storage element 307 at time t8. The diagram also shows the state of each output signal of each circuit element in each time area as of the corresponding discrete time.

Thus when a user sees an error in the output of element 307 at time t8, the can ask LIU's system to generate the temporal schematic diagram display of FIG. 5. However, when the user is initially interested in initially determining whether the outputs of storage elements 304-305 are of the correct states at time t7, it is necessary for the user to manually trace the schematic diagram of time area t7 back to those storage elements to determine their states. This may not be too difficult to do for the simple schematic diagram of FIG. 5, but can be much more difficult, time-consuming and prone to human error for more complex schematic diagrams.

The applicant's method, as recited in claim 25 makes the debugging process easier for the user by initially generating a less complex display of relevant signals states and times, as illustrated for example in the applicant's FIG. 6. When the applicant selects a storage element output signal and a discrete time, such as signal R1 at time 90, the method generates a display containing two columns of symbols. The first column, corresponding to the selected "first discrete time" 90, includes a symbol representing the state of a selected "first signal" R1 at the selected "first discrete time" 90 and excludes symbols representing any other signal states. The second column, corresponding to a next preceding "second discrete time" 80, includes symbols representing states at time 80 only of a first set of signals R2 and R3. The first set of signals is selected to include all signals of the circuit other output signals of unclocked elements having states at time 80 that can affect the state of the first signal R1 at time 90.

Thus the user can immediately determine the state of every storage element output signal or circuit input signal at time 80 that could have influenced the state of the selected first signal R1 at time 90. Therefore it isn't necessary for the user to manually trace signal paths of a schematic diagram of the type taught by LIU in order to determine the states of signals R2 and R3.

The applicant's claim 25 is therefore patentable of LIU because LIU does not teach the recited step c, since LIU's display does not arrange symbols indicating signal states into columns in the manner recited in the claim.

Claim 26.

Claim 26 depends on claim 25 and is patentable over LIU for similar reasons. Claim 26 further recites "the display excludes any schematic diagram representation of any portion of the circuit." Claim 26 is further patentable over LIU because LIU includes schematic diagram representations of portions of the circuit.

Claim 27

Claim 27 depends on claim 25 and is patentable over LIU for similar reasons.

Claim 28.

Claim 28 depends on claim 25 and is patentable over LIU for similar reasons. Claim 28 further recites method steps by which the user can, for example, alter the display of FIG. 6 (produced in accordance with claim 25) to look like the display of FIG. 7. In particular, when the user selects signal R2 and time 80, a second set of signals R4 and R5 whose state at time 70 affect the state of signal R2 are identified, and a third column of symbols indicating states of those two signals at time 70 are added to the display. LIU does not teach this sort of incremental addition to a display, and does not teach aligning symbols representing signals states at particular discrete times into columns.

Claim 29

Claim 29 depends on claim 28 and is patentable over LIU for similar reasons. Claim 29 further recites "the user selects said one

of the signals of the first set as a second signal and selects the second discrete time by selecting the symbol for the second signal in the second column." For example, the user selects signal R2 and time 80 of FIG. 6 by mouse clicking on the symbol for symbol R2, thereby causing the system to alter the display to appear as in FIG. 7. LIU does not teach this.

Claim 30

Claim 30 depends on claim 28 and is patentable over LIU for similar reasons.

Claim 31

Claim 30 depends on claim 30 and is patentable over LIU for similar reasons. Claim 31 further recites method steps by which the user can, for example, alter the display of FIG. 7 (produced in accordance with claim 28) to look like the display of FIG. 8. In particular, when the user selects signal R3 and time 80, a third set of signals R1 and R5 whose state at time 70 affect the state of signal R3 are identified, symbols indicating states of those two signals at time 70 are added to the third column. LIU does not teach this sort of incremental addition to a display, and does not teach aligning symbols representing signals states at particular discrete times into columns.

Claim 32

Claim 31 depends on claim 30 and is patentable over LIU for similar reasons and for reasons expressed above in connection with claim 29.

Claim 33

Claim 3 depends on claim 31 and is patentable over LIU for similar reasons. Claim 3 further recites responding to a user command by adding fly-lines to the display to indicate dependency relationships between signals of the first and second columns as illustrated for example in FIG. 10. LIU does not teach this.

Claim 34

Claim 34 depends on claim 33 and is patentable over LIU for similar reasons. Claim 34 further recites identifying each signal of the second set that changed state from the third discrete time to the second discrete time, and altering the display to visually distinguish every fly line in the display that connects the symbol in the second column corresponding to an identified signal of the second set to the symbol in the first column from every other fly line in the display. LIU does not teach this.

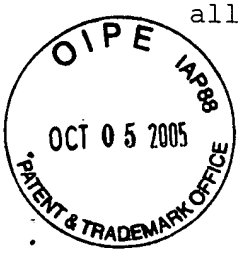
Claim 35

Claim 35 is somewhat similar to claim 25, except that it relates to a method by which a user can direct creation of a "fan-out" display as illustrated, for example, in FIG. 15 rather than a "fan-in" display as illustrated, for example, in FIG. 9. Per step a, the user initially selects a circuit signal and time, such as for example signal R6 at time 10 and. per steps b and c the system creates a display having two columns of symbols, including a first column having the symbol indicating state of the signal R6 at time 10, and a second column having a symbol for every register output signal whose state at a next discrete time 20 is affected by the state of signal R6 at time 10. LIU does not teach generating such a two-column fan-out display.

Claims 36-43

Claims 36-43 depend on claim 35 and are patentable over LIU for similar reasons and for reasons analogous to those expressed above in connection with claims 2-8, respectively.

It is believed that the application is in condition for allowance. Notice of allowance is therefore respectfully requested.



Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: NOVA 2198
Postcard: 10/05-1

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Lindsay Stockwell